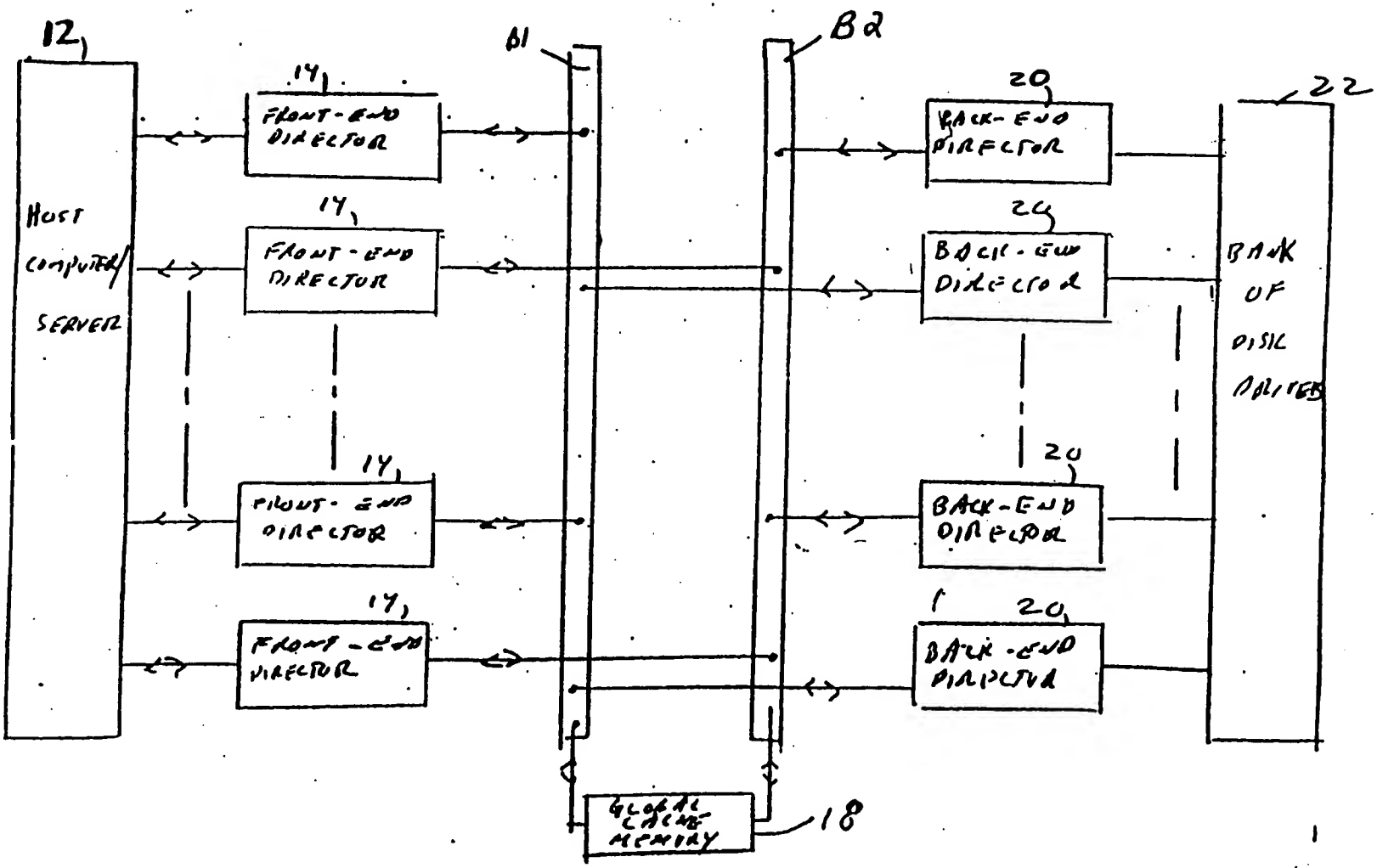
Christopher S. MacLellan
CYCLIC REDUNDANCY CHECK (CRC)
PARITY CHECK SYSTEM AND METHOD
Application No. 09/746,174

FIG. 1
PRIOR ART



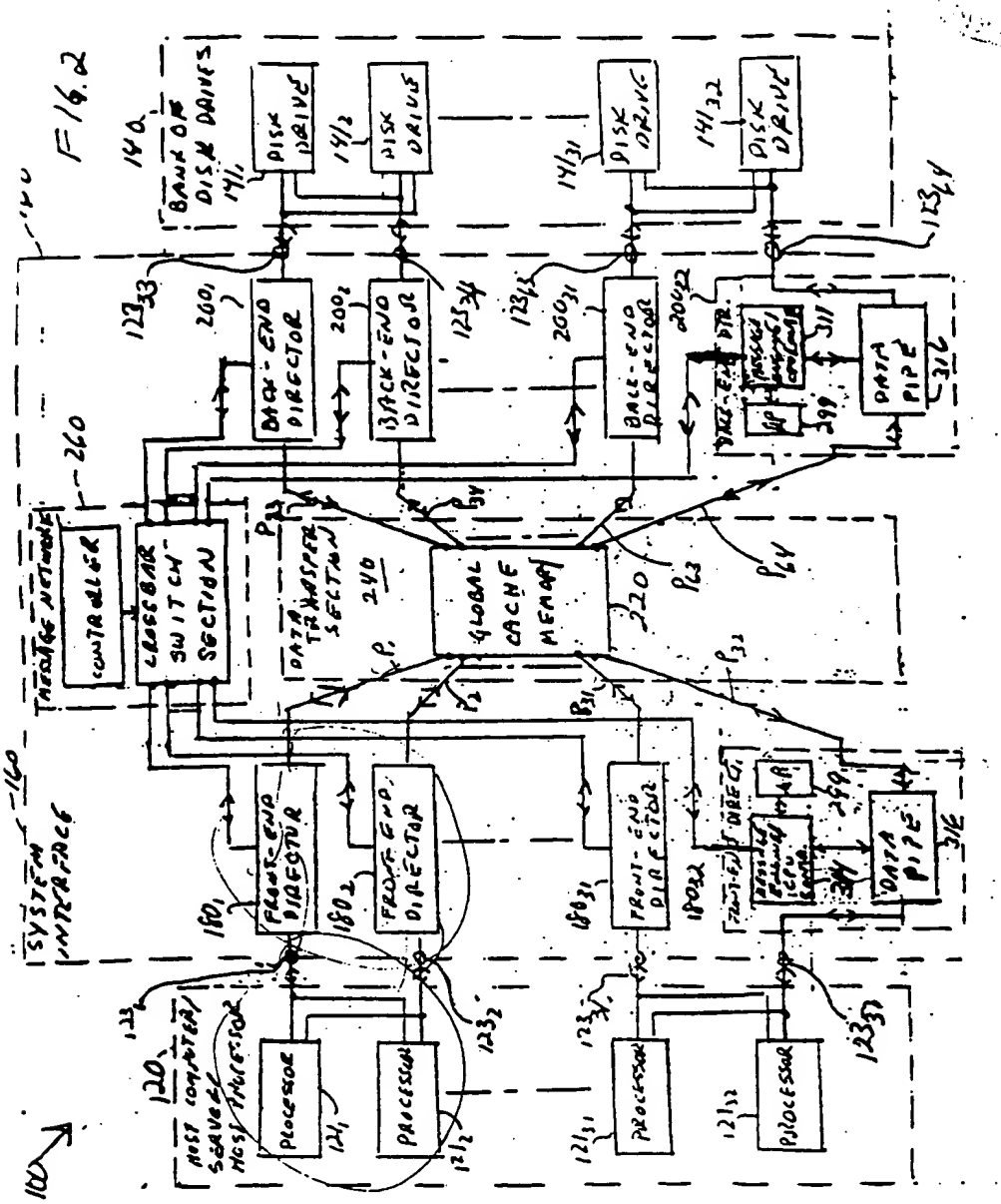


FIG. 2
100
120
140
160
180
200
220
240
260
300
310
312
314
316
DISK DRIVES
DISK DRIVE
BACK-END DIRECTOR
FRONT-END DIRECTOR
GLOBAL CACHE MEMORY
DATA TRANSFER SECTION
CROSSBAR SWITCH SECTION
CONTROL
DATA PIPE
PROCESSOR
SYSTEM INTERFACE

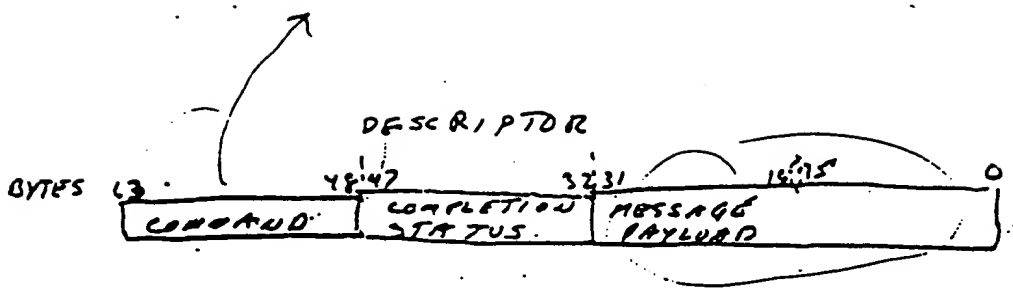

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

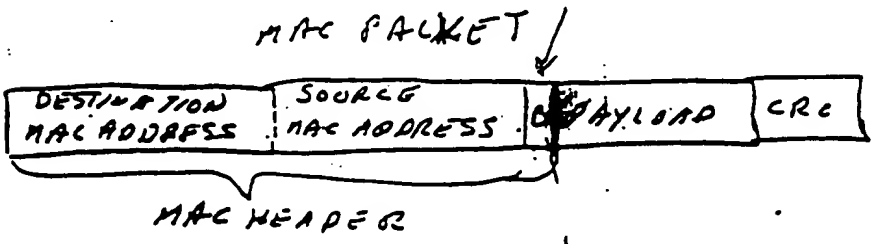

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

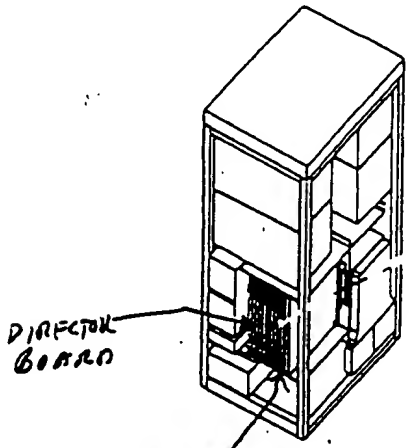

DIRECTOR BOARD
CACHE MEMORY 220

FIG 3

FIG 4

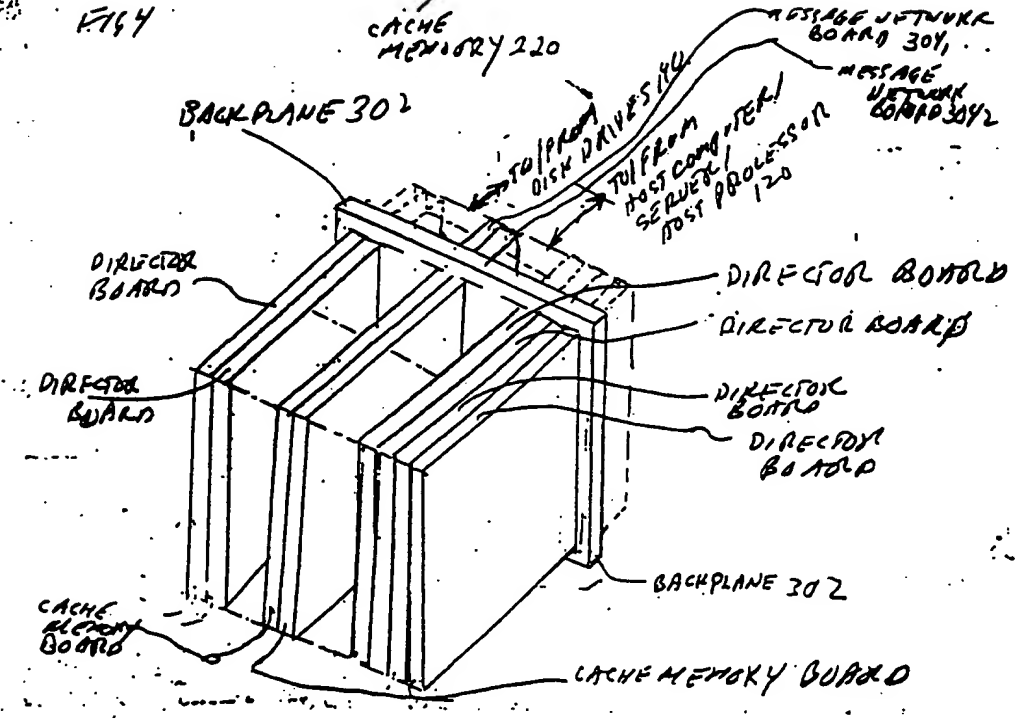
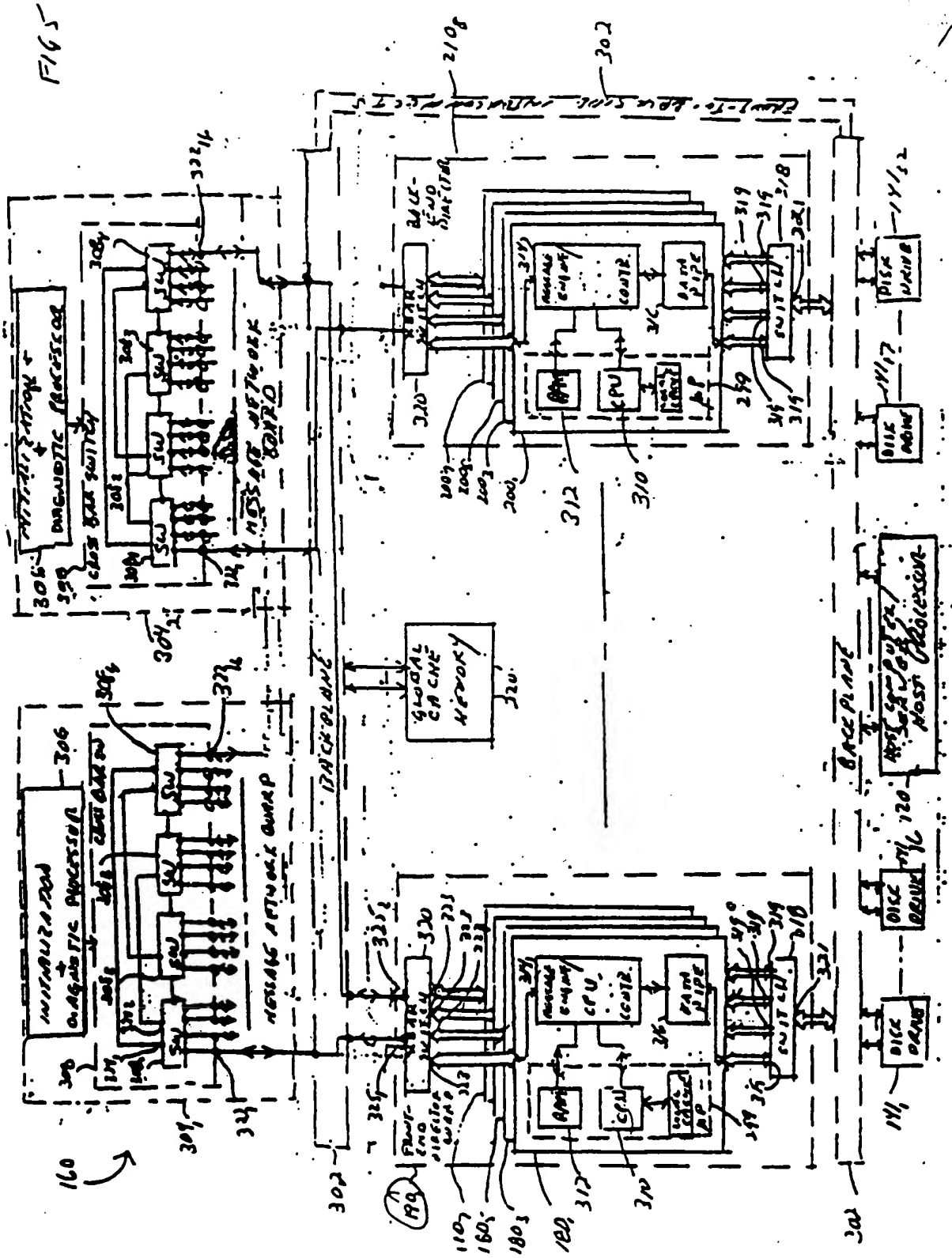
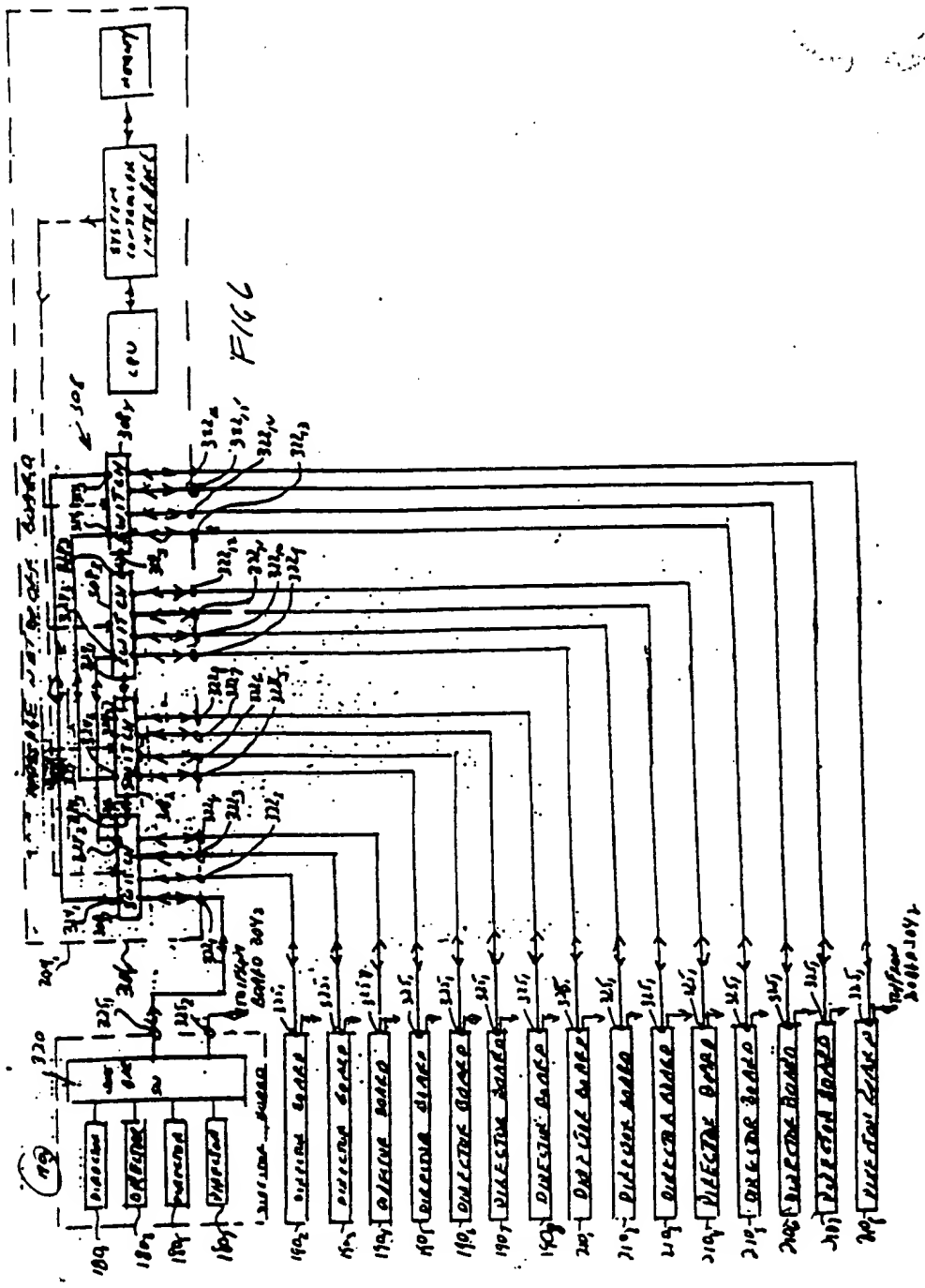

BACKPLANE 302
TO/FROM DISK DRIVES 114
TO/FROM HOST COMPUTER/ SERVER/ HOST PROCESSOR 120
MESSAGE NETWORK BOARD 304
MESSAGE NETWORK BOARD 304
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

FIG 5





FOSTER-MILLER

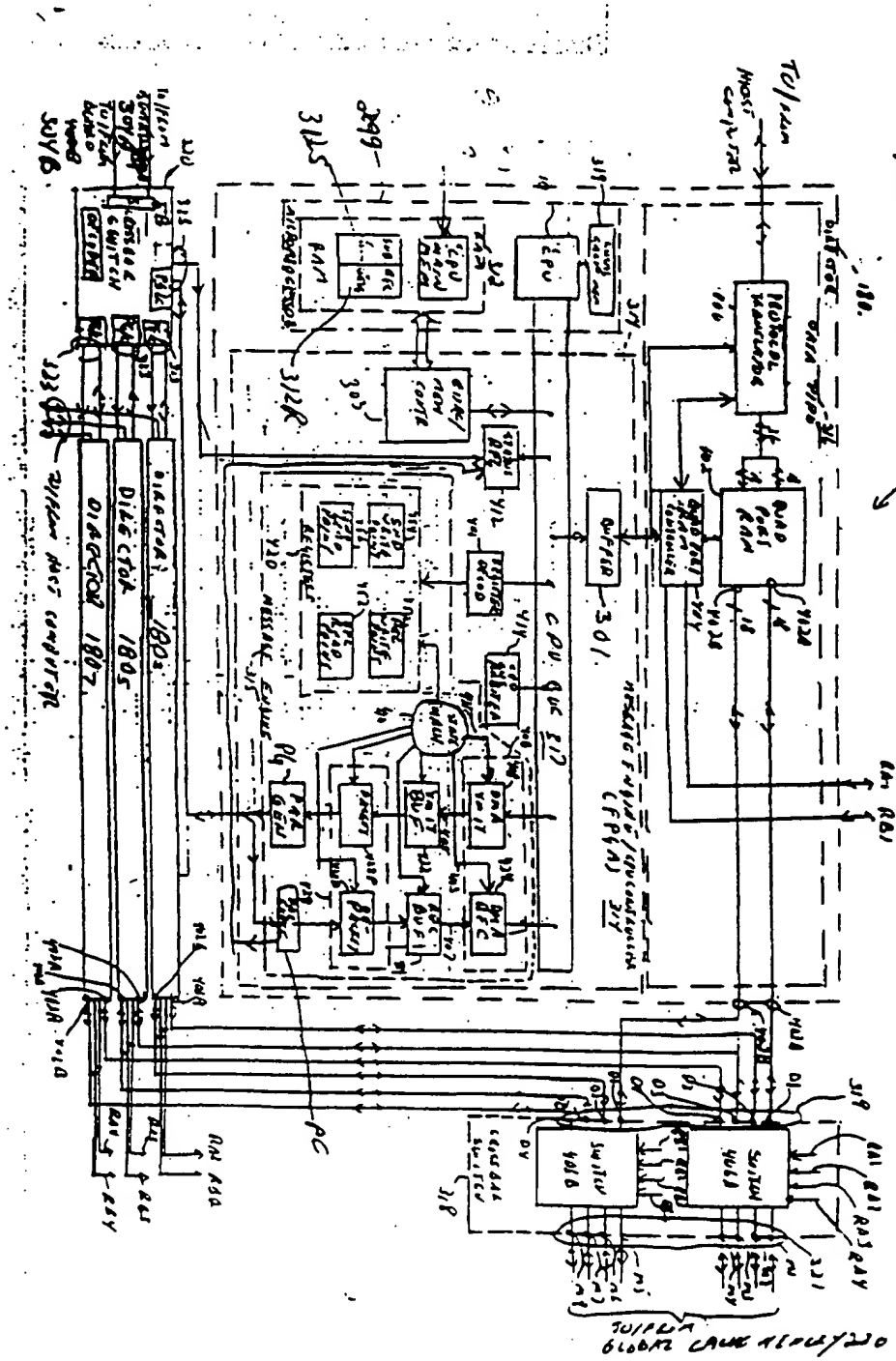


FIG. 7

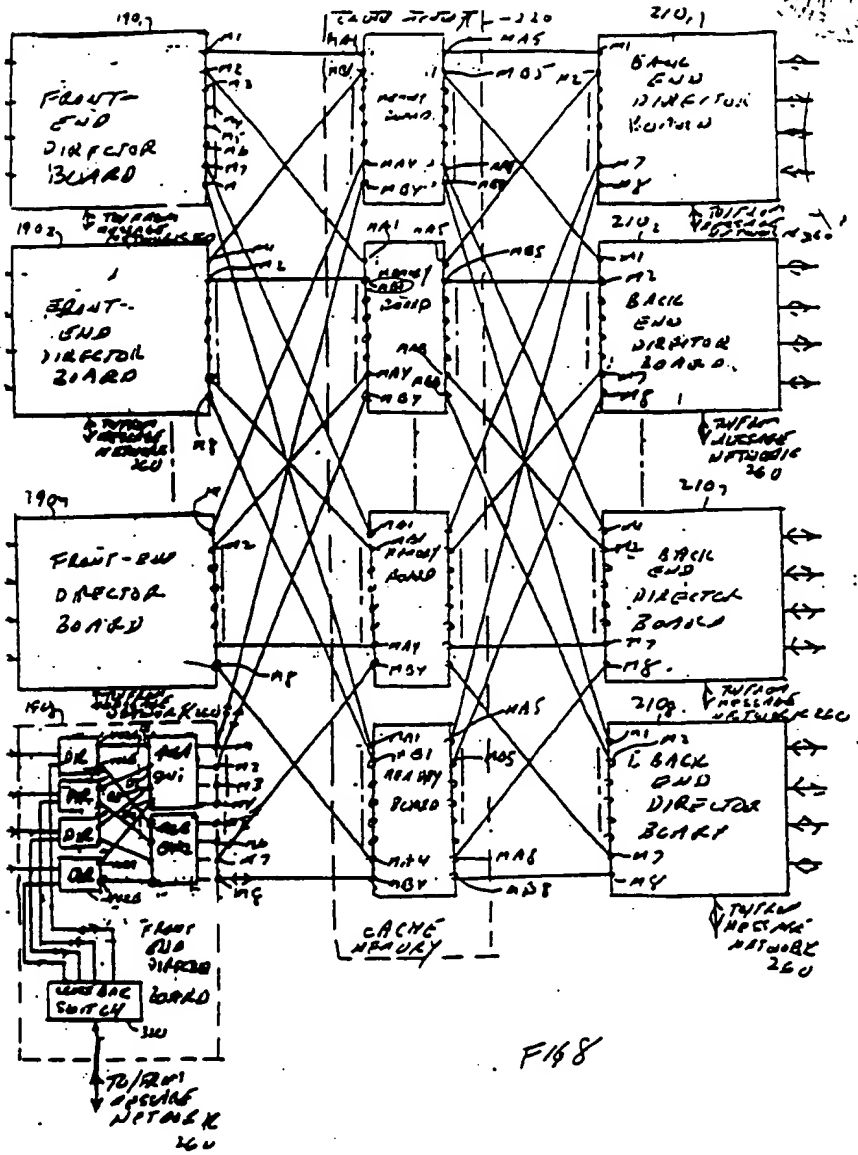


FIG 8

EMC-01-074-US

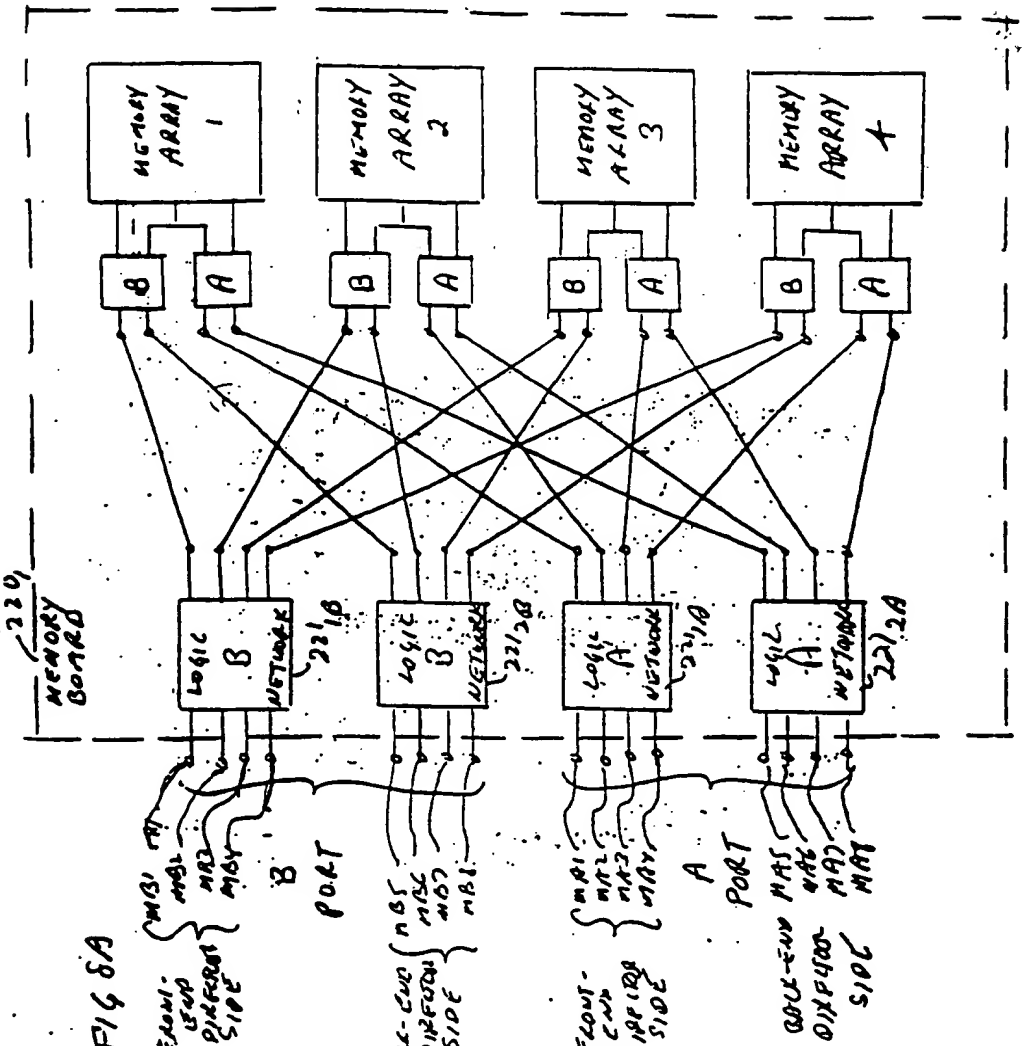

MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
220
MEMORY BOARD
LOGIC B NETWORK
221/1B
LOGIC B NETWORK
221/2B
LOGIC A NETWORK
221/1A
LOGIC A NETWORK
221/2A
B PORT
A PORT
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE

FIG 8A

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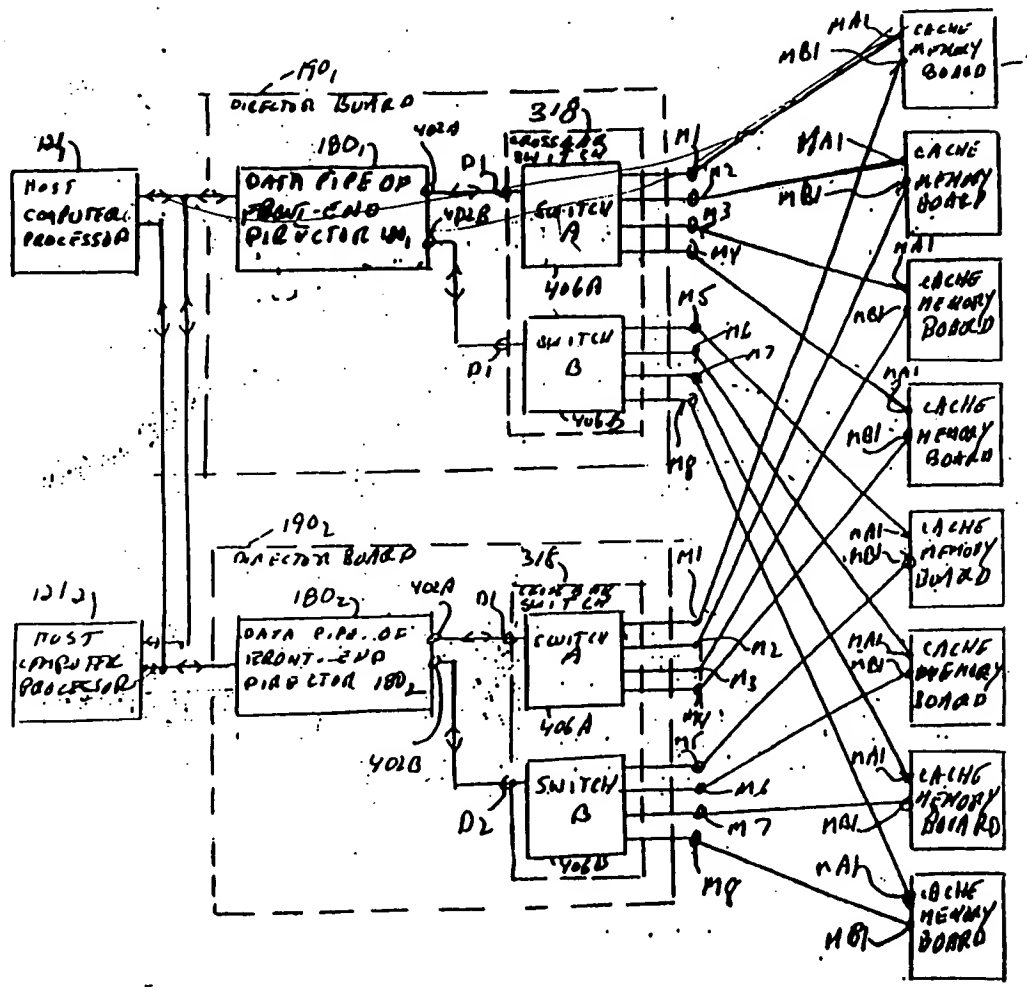


FIG 8B

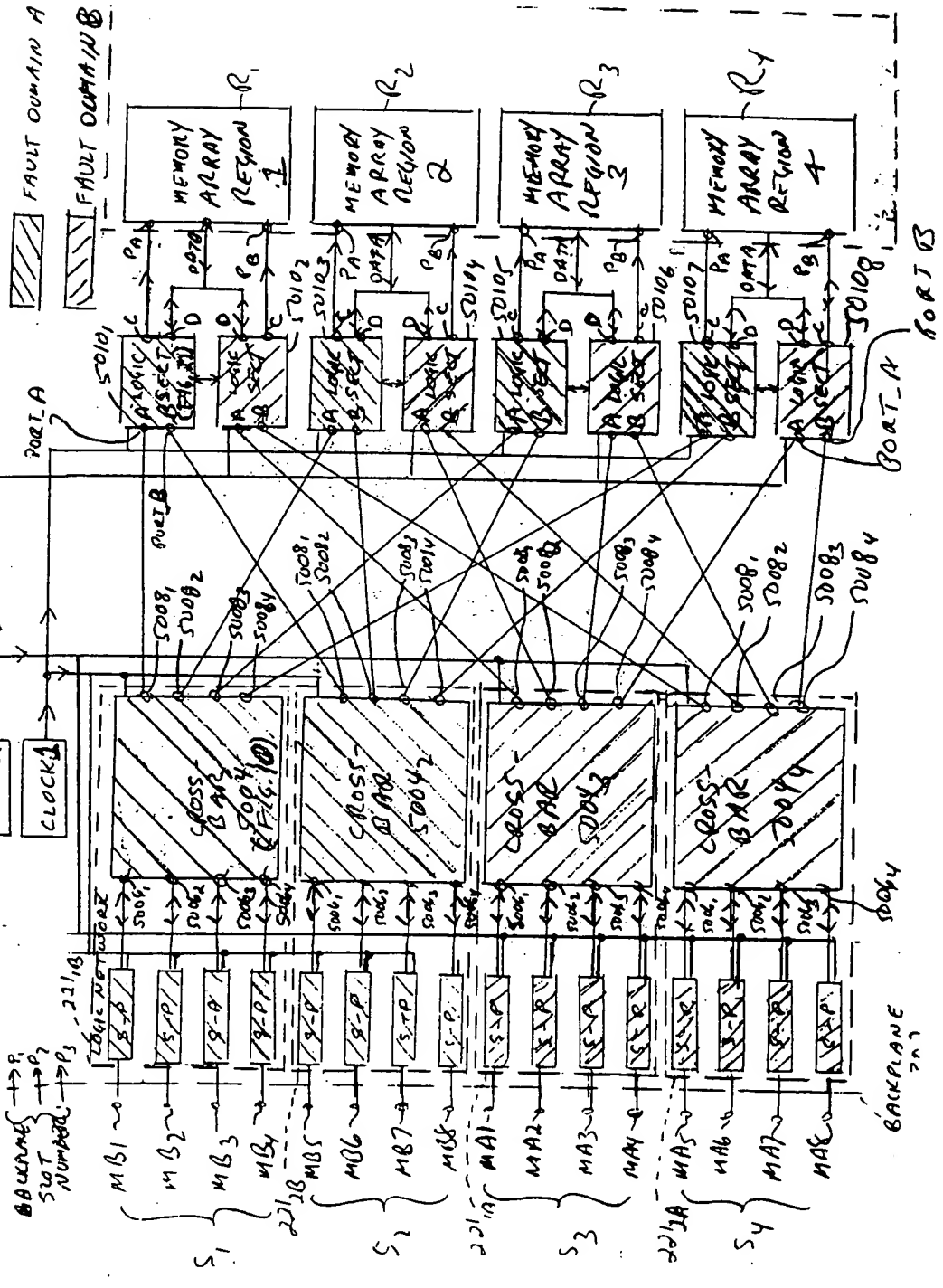

FAULT DOMAIN A
FAULT DOMAIN B
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
PORT_A
PORT_B
CLOCK2
CLOCK1
CROSS BAR SD04
CROSS BAR SD04
CROSS BAR SD04
CROSS BAR SD04
BACKPLANE

FIG. 9

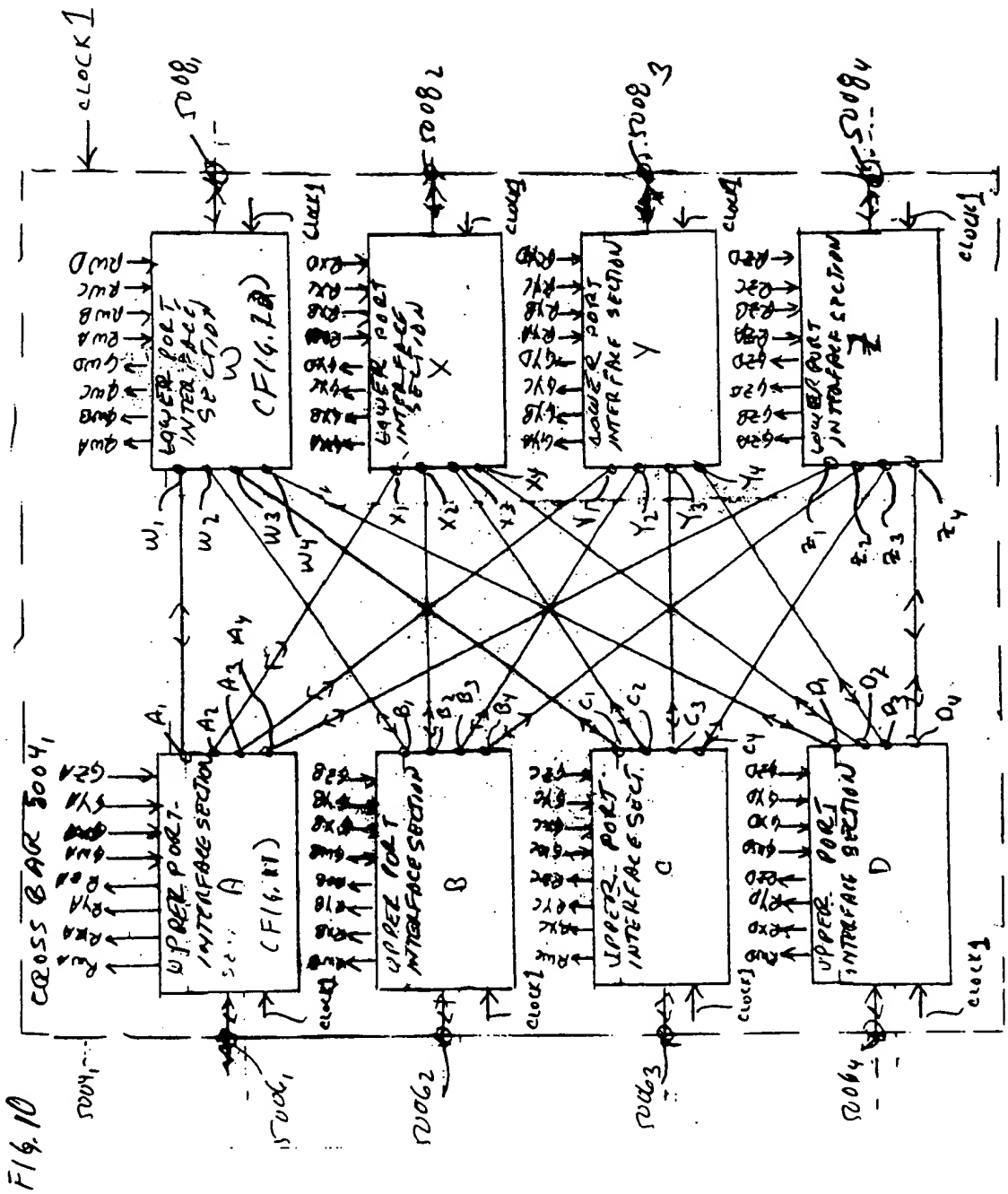

CROSS BAR SOC4
CLOCK 1
SOB1
SOB2
SOB3
SOB4
UPPER PORT INTERFACE SECTION A
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECT. C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
SOA1
SOA2
SOA3
SOA4

FIG. 10

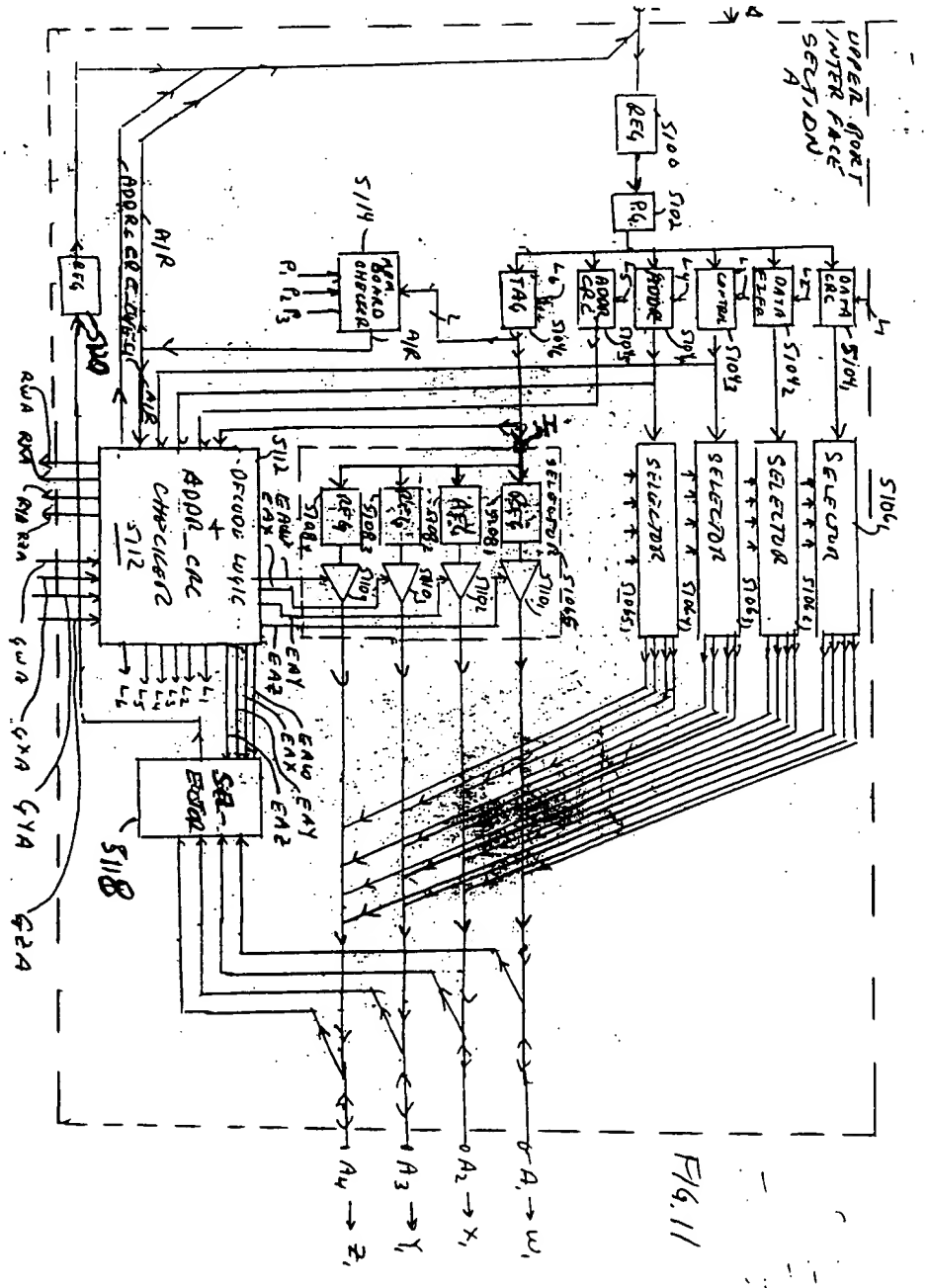

UPPER PORT INTER FACE SELECTION A
REG
S100
S102
PG
S114
HAMMING ENCODER
P1 P2 P3
A/R
ADDRESS OR CONTROL
TAG
ADDR CRC
ADDR
CONTROL
DATA BYTE
DATA CRC
S104
S106
S108
S110
S112
S116
S118
SELECTOR
SEL ECTOR
SELECTOR
SELECTOR
DECODE LOGIC + ADDR_CRC CHECKER
SEL ECTOR
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

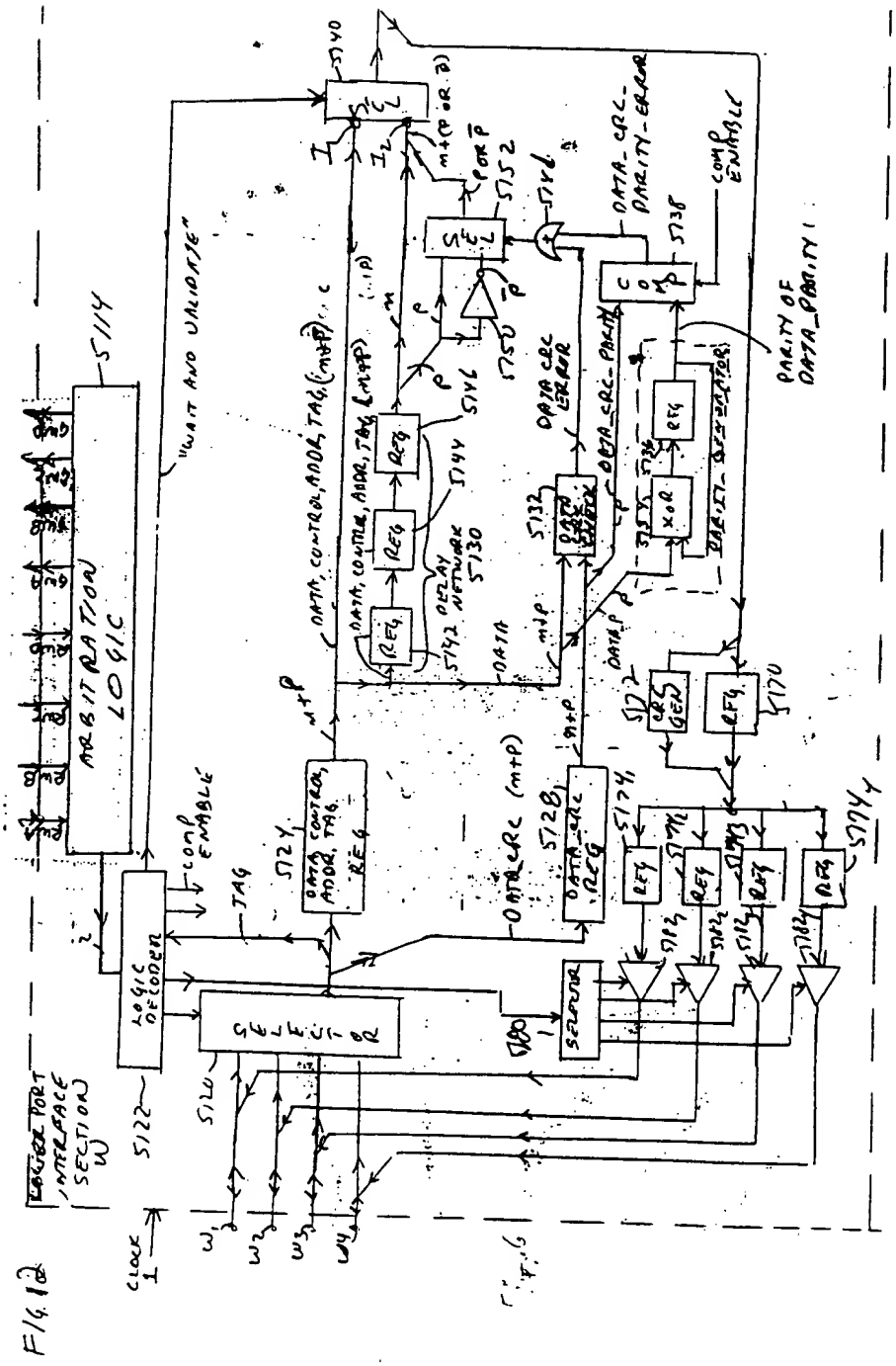

LOGIC DECODER
SELECTOR
DATA CONTROL ADDR. TAG REG
DATA, CONTROL, ADDR, TAG (m+p)
DELAY NETWORK
DATA
DATA CRC ERROR
DATA_CRC_PARITY
DATA_CRC_PARITY_ERROR
COMP ENABLE
PARITY OF DATA_PARITY
WAIT AND UNLOAD
TAG
COMP ENABLE
DATA CRC (m+p)
REG
XOR
CRC GEN
SELECTOR
CLOCK

FIG. 12

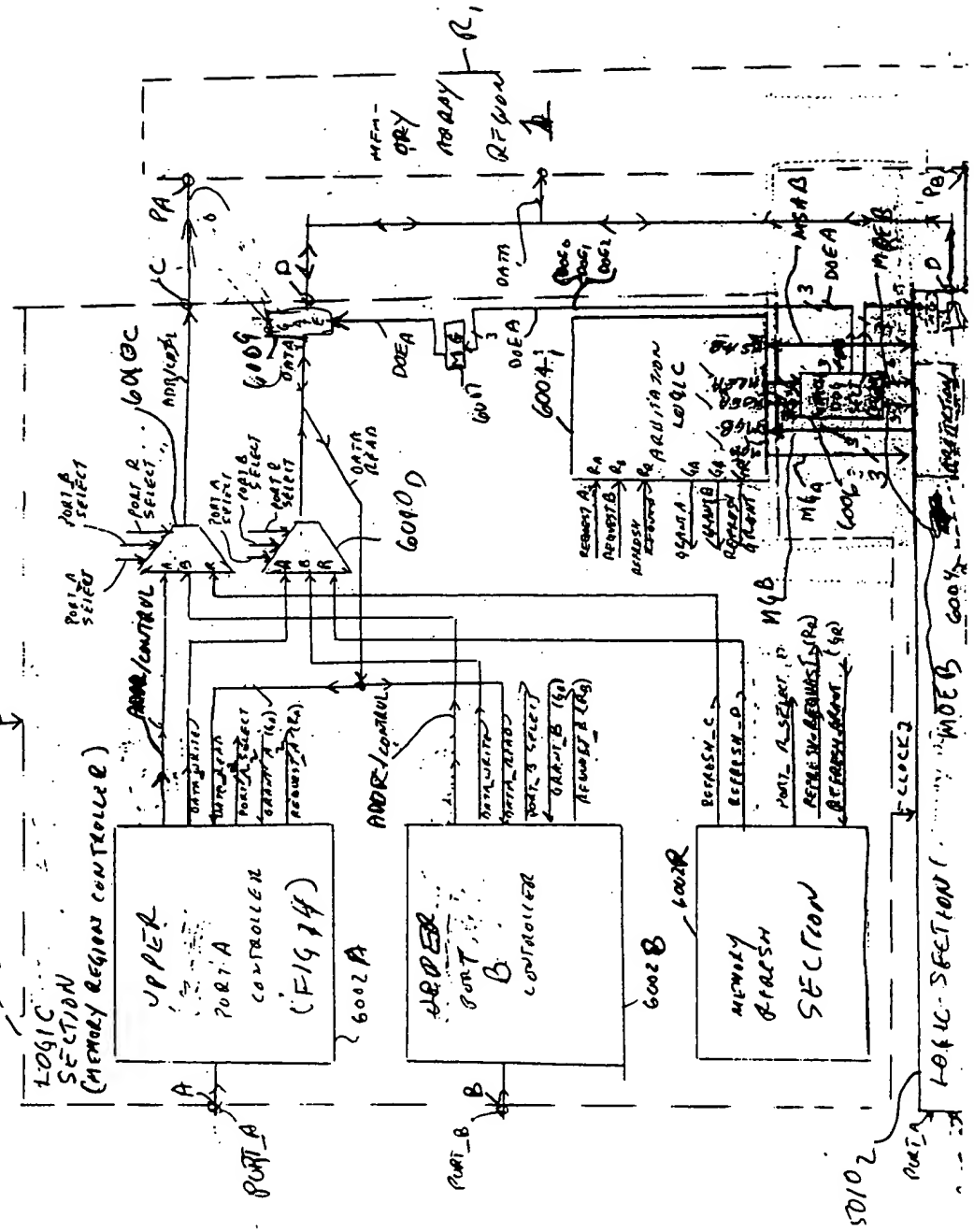


FIG. 1B
LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
CLOCK1
UPPER PORT A CONTROLLER (FIG 1A)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY ARRAY SECTION
6002C
PORT_A
PORT_B
5012
CLOCK2
MODE
6004
6006
6008
6009
6010
ADDR/CONTROL
DATA READ
DATA WRITE
REFRESH_C
REFRESH_D
ARBITRATION LOGIC

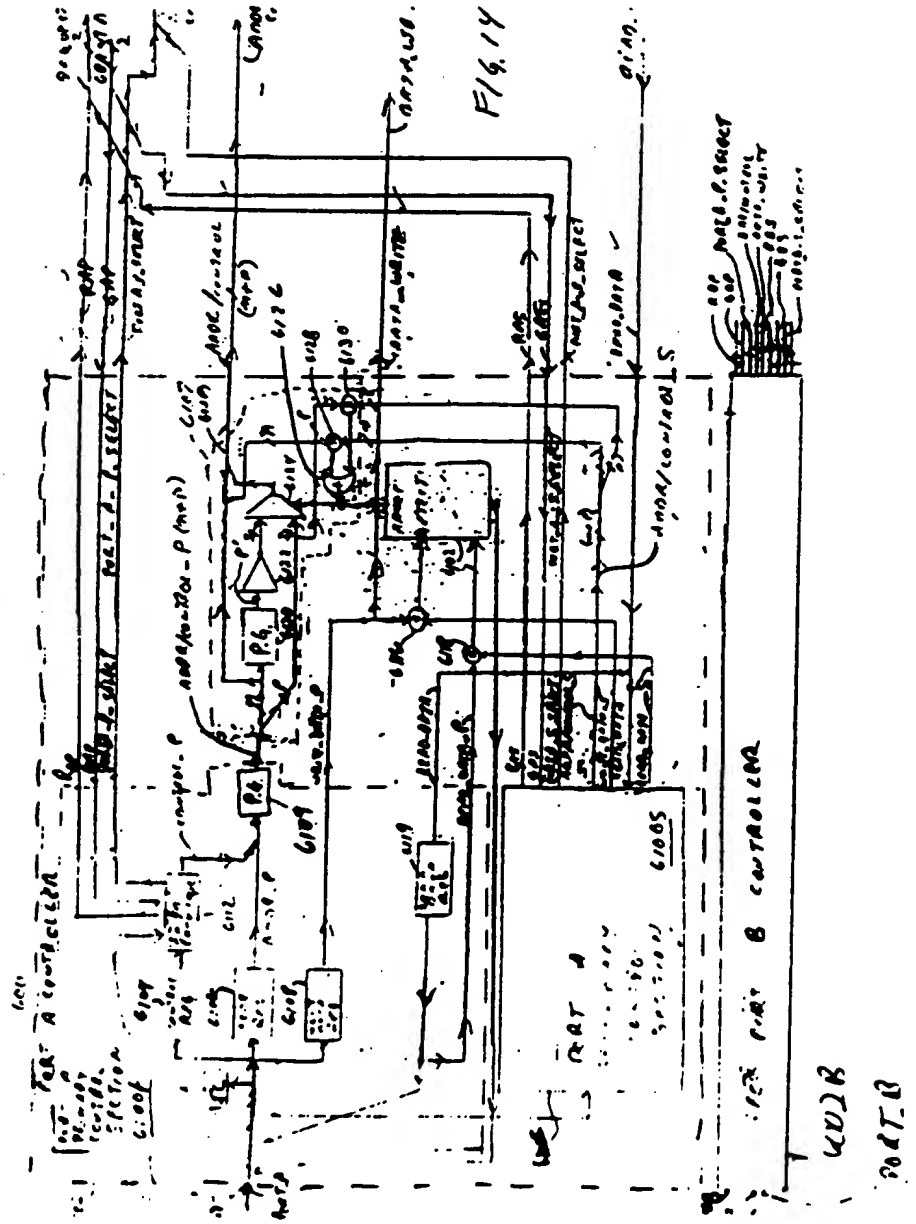


FIG. 14

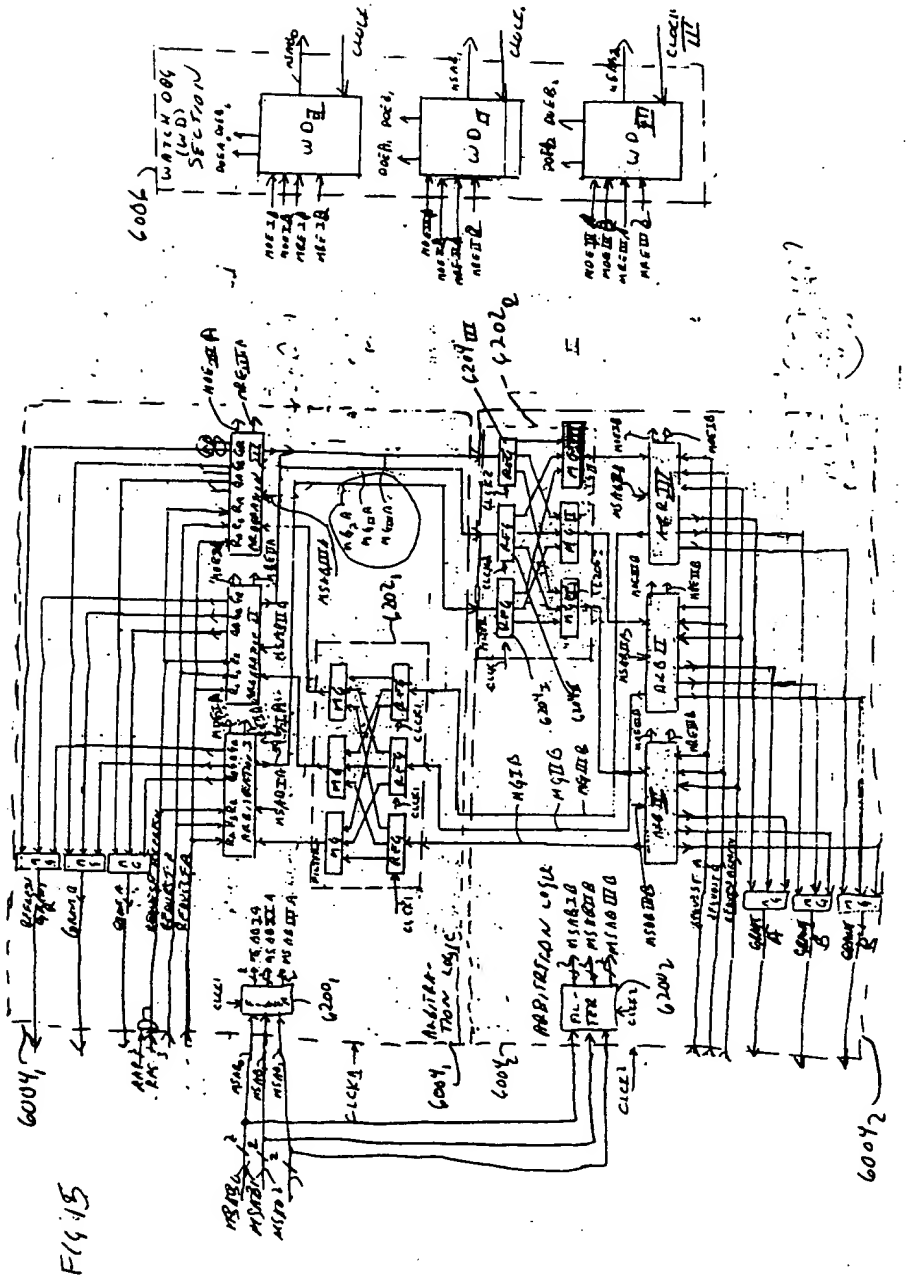


Fig. 7B

T020h0" h2T9h260

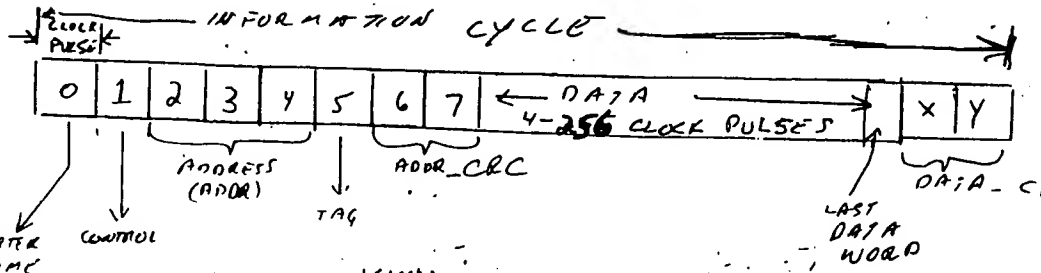


FIG. 16

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

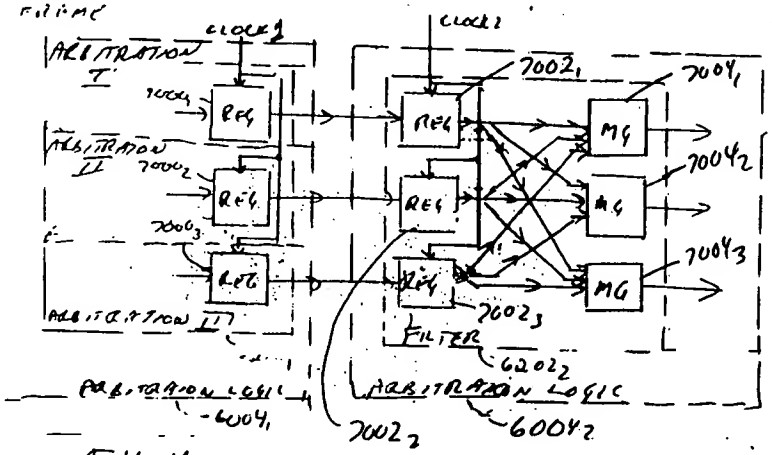
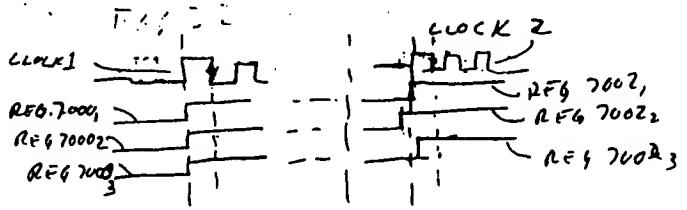


FIG. 18

FIG. 19



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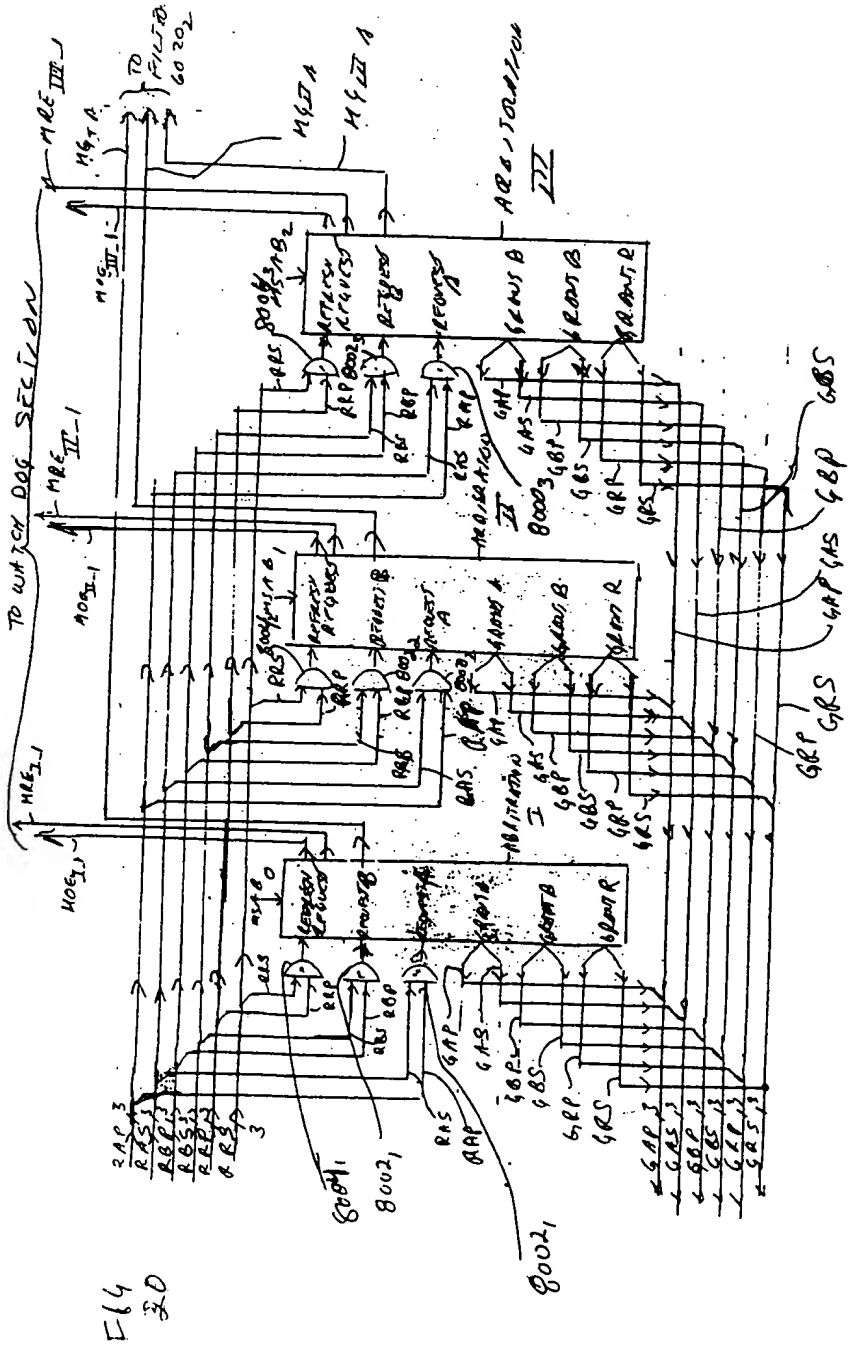
TO WATCH DOG SELECTOR
MUX III
MUX II-1
MUX II-1
MUX I-1
MUX I-1
TO FIELD 60 202
HOST A
HOST A
HOST A
ADDRESS TRANSLATION III
ADDRESS TRANSLATION II
ADDRESS TRANSLATION I
8002
8002
8002
8002
8002
GAP
GAS
GBP
GBS
GRP
GRS

FIG 30